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Cascaded H-bridge Multilevel Inverter for Photovoltaic Applications

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ABSTRACT

In this work, a novel single-phase cascaded multilevel inverter is proposed based on the H-bridge units. The proposed topology increases the output voltage levels by reducing the power electronic devices such as switches, power diodes, dc voltage sources and driver circuits that help to reduce the inverter cost and installation space. This topology not only reduces the number of power electronic devices but also reduces the amount of voltage blocked by the switches. This advantage is due to the developed H-Bridge. Normally, a single conventional H-bridge can generate 3 levels at the output, which utilizes 4 power electronics switches and 2 dc voltage sources. When three conventional H-bridge are connected in series, it can generate 7 levels in the output. This conventional circuit utilizes 12 switches and 3 dc voltage sources. In order to reduce power electronics devices, conventional H-bridge is modified with 6 switches and 2 DC voltages. This developed H-bridge can generate 7 levels atthe output. In this case, utilization of switches and the dc voltage source get reduced. By using this topology, it is conceivable to generate any number of levels at the output with a minimum number of power electronic devices.

1. Introduction

In recent days, the multilevel inverter is widely used due to their benefits such as high power quality, lower switching losses, lower dv/dt and reduced harmonics distortion. The multilevel inverter is of three types: Diode clamp multilevel inverter, Flying capacitor multilevel inverter and cascaded multilevel inverter(Zamiri et al, 2016), (Ajami et al, 2014). Among these three types, Cascaded multilevel inverter is advantageous due to its modularity and simplicity of control. The cascaded multilevel inverter is classified into two types: symmetric and asymmetric cascaded multilevel inverter. In this, the symmetric cascaded multilevel inverter has an equal magnitude for DC voltage source while the asymmetric cascaded multilevel inverter has an unequal magnitude for dc voltage source. In order to generate more levels at the output, magnitude of the dc voltage source can be increased. The cascaded multilevel inverter with two different algorithms as symmetric and asymmetric inverters has been presented by (Imarazene et al, 2017). In the symmetric cascaded multilevel inverter, DC voltage sources with same voltage amplitudes are used but consumption of power electronic devices to generate the specific level of output tremendously gets increased (Babaei 2014).The main advantage of these inverters is the low numberof different voltage amplitudes of the used DC sources. However, higher number of required power electronic devices, power diodes and driver circuits in generating a specific output level are their disadvantages (Ebrahimi et al, 2012). In order to increase the number of output levels with a lower number of power electronic devices, different asymmetric cascaded multilevel inverters have been presented (Babaei, 2008).

In this paper, a novel single phase cascaded multilevel inverter with a series connection of H-bridge units is proposed in order to reduce the power electronic devices such as switches, power diodes, power supply and the driver circuits. The performance of the proposed cascaded multilevel inverter is analyzed by comparing the results obtained with the conventional cascaded multilevel inverter. In this paper, seven levels are generated at the output by a single developed H-Bridge and 13 levels are generated at the output by cascading two developed H-Bridge.

1. Methods

2.1 Conventional topology

The concept of the cascaded multilevel inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each H-bridge (Babaei et al,2015). An 'n' level cascaded H-bridge multilevel inverter needs 2(n-1) switching devices and m voltage sources in order to generate 2m+1 output voltage levels. Here m denotes the number of H-bridge and n denotes the number of outputlevels.

Figure 1 shows the circuit diagram of the conventional H-bridge. It consists of four power electronic switches and one DC voltage source. It can generate three levels at the output.When three conventional H-bridges are connected in the series, it can generate seven levels at the output. The circuit utilizes 12 switches and three DC voltage sources.

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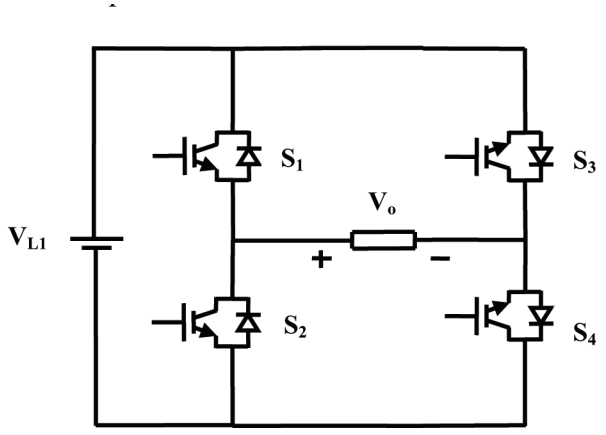

Figure 1 Conventional H-bridge

Table 1 Output voltage of the developed H-bridge based on different switching pattern

State	S_1	S_2	S_3	S_4	S_5	S_6	V_o
1.	1	0	0	1	0	1	V_{L1}
2.	0	1	1	0	0	1	V_{R1}
3.	1	0	1	0	0	1	$V_{L1}+V_{R1}$
4(a).	1	0	1	0	1	0	0
4(b).	0	1	0	1	0	1	0
5.	0	1	1	0	1	0	$- V_{L1}$
6.	1	0	0	1	1	0	$- V_{R1}$
7.	0	1	0	1	1	0	$-[V_{L1}+V_{R1}]$

2.2 Proposed topology

Figure 2 shows the developed H-bridge unit. The developed H-bridge unit consists of six unidirectional power switches and two isolated dc voltage sources (V_{L1} and V_{R1}). The main disadvantage of the proposed H-bridge over the conventional H-bridge is that the proposed H-bridge requires more switches and DC voltage sources compared to conventional H-bridge. Even though the higher number of switches and dc voltage sources are used, it can generate seven levels at the output whereas the conventional H-bridge can generate only three levels at the output**.**Table 1 shows the different output levels generated by the developed H-bridge due to different switching patterns. In this table, 1 represents the ON state of the switch and 0 represents the OFF state of the switch. Due to appropriate switching of the developed H-bridge, it can generate seven levels (3 positive level, 3 negative level and 1 zero level) at the output. In order to generate required levels at the output, one power switch from each is turned on during each switching patterns (Lupon et al,2014). Device to be turned on and off are chosen based on output levels required.

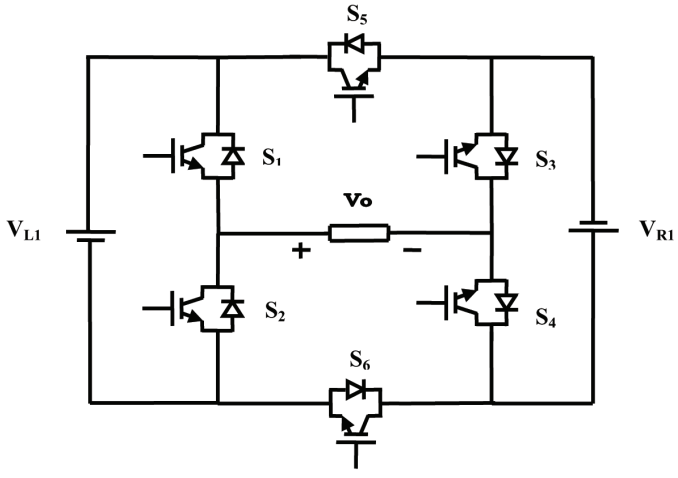

Figure 2 Developed H-bridge

In order to attain seven levels at the output, the magnitude of two dc voltage sources (V_{L1} and V_{R1}) areequal, the proposed topology can generate only five levels at the output. Therefore, in order to generate a higher number of levels at the output, magnitude of the DC voltage sources should be selected differently (Babaei, 2013).A cascaded multilevel inverter can be constructed by connecting the 'n' number of H-bridge units in series. Figure 3 shows the cascaded multilevel inverter with a series connection of H-bridge units. This topology can generate thirteen levels at the output. Like the seven level inverter, the output levels of the 13 level inverter depends on the different switching pattern employed (Matsumoto et al, 2017).

In the proposed cascaded multilevel inverter topology, the required number of switches (N_{switch}), IGBT's (N_{igbt}), dc voltage source (N_{source}) and the driver circuit (N_{driver}) are calculated by using the formula given below

$$N_{switch} = N_{igbt} = N_{driver} = 6n$$

$$N_{source} = 2n$$

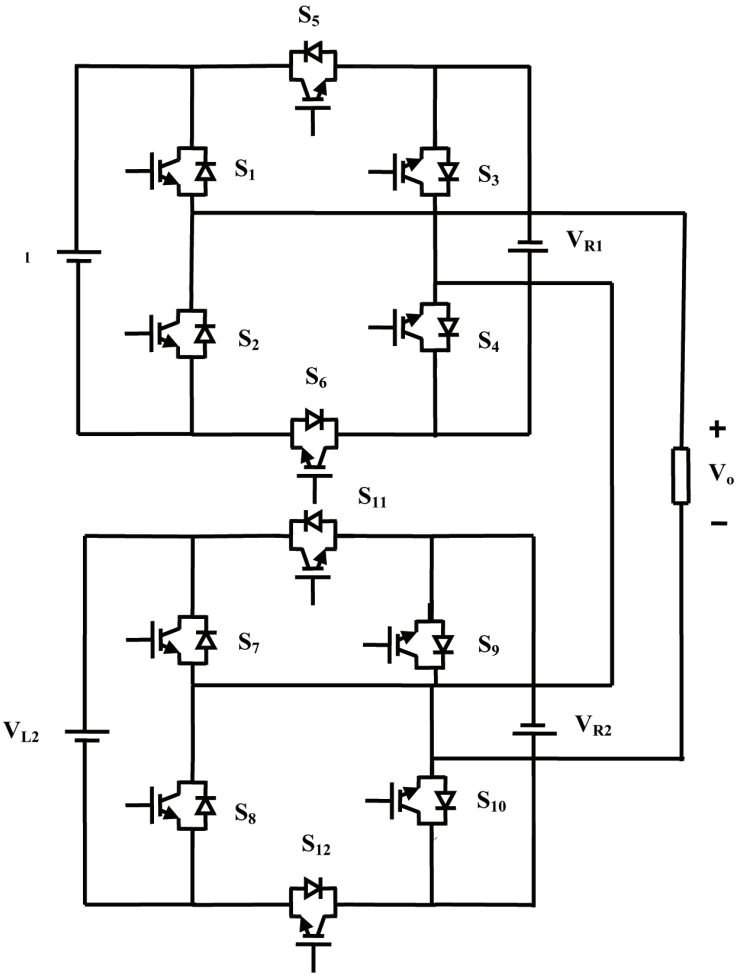

Figure 3 Proposed cascaded multilevel inverter

The voltages blocked by the switches S_1 and S_2 are givenby

$$Vs_1=Vs_2=V_{L1}$$

where Vs_1 and Vs_2represent the amount of blocked voltage by the switches S_1 and S_2respectively. The voltage blocked by the switches S_3 and S_4 are givenby

$$Vs_3=Vs_4=V_{R1}$$

where Vs_3 and Vs_4represent the amount of blocked voltage by switches S_3 and S_4respectively.The voltage blocked by switches S_5 and S_6 are given by

$$Vs_5=Vs_6=V_{L1}+V_{R1}$$

where Vs_5 and Vs_6represent the amount of blocked voltage by switches S_5 and S_6 respectively.

Therefore, the amount of voltage blocked by all the switches in the proposed unit is given by

$$V_{block}= 4(V_{L1}+V_{R1})$$

Thus the maximum value of voltage blocked by all the switches in the 13 level inverter is given by

$$V_{block}=4 (V_{L1}+V_{R1}+V_{L2}+V_{R2})$$

Table 2 shows the switching sequence of 13 level inverter. In the table, 1 represents the

ON state of the switch and 0 represents the OFF state of the switch respectively.

Table 2 Output voltage of the proposed multilevel inverter

S.No	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	Output
1.	1	0	0	1	0	1	1	0	1	0	1	0	V_{L1}
2.	0	1	1	0	0	1	1	0	1	0	1	0	V_{R1}
3.	1	0	1	0	0	1	1	0	1	0	1	0	$V_{L1}+ V_{R1}$
4.	1	0	0	1	0	1	1	0	0	1	0	1	$V_{L1}+V_{L2}$
5.	0	1	1	0	0	1	0	1	1	0	0	1	$V_{R1}+V_{R2}$
6.	1	0	1	0	0	1	1	0	1	0	0	1	$V_{L2}+ V_{R2}$
7(a).	1	0	1	0	1	0	1	0	1	0	1	0	0
7(b).	0	1	0	1	0	1	0	1	0	1	0	1	
8.	0	1	1	0	1	0	0	1	0	1	0	1	$- V_{L1}$
9.	1	0	0	1	1	0	0	1	0	1	0	1	$- V_{R1}$
10.	0	1	0	1	1	0	0	1	0	1	0	1	$- V_{L1}- V_{R1}$
11.	0	1	1	0	1	0	0	1	1	0	1	0	$- V_{L1}- V_{L2}$
12.	1	0	0	1	1	0	1	0	0	1	1	0	$- V_{R1}- V_{R2}$
13.	0	1	0	1	1	0	0	1	0	1	1	0	$- V_{L2}- V_{R2}$

When the device is switched, the sequence given in Table 2, 13 levels are obtained at the output.

In order to generate all possible voltage levels at the output, nine different algorithms are proposed to determine the different magnitude of dc voltage sources (Ebrahim et al, 2014). Each proposed algorithm has a different number of voltage levels at the output, maximum voltages blocked by the switches differ and have the different magnitude for dc voltage source and different output amplitudes (Waltrich et al,2010, Prayag et al, 2017).

2.3 Comparing proposed topology with the other topologies

The main objective of the proposed multilevel inverter is to increase the output voltage level by reducing the power electronic devices. The proposed topology is compared in terms of components [power electronic switches, diodes, DC sources] with conventional and other similar topologies are available in the literature.

2.3.1 Conventional topology

From the table 3a, it is clear that the conventional topology uses 2(m-1) power electronic switches, (m-1)/2 separate DC sources in order to generate 2s+1. Due to the useof 2(m-1) power electronic switches and (m-1)/2 DC sources, the size of the inverter and the losses due to the switchesincreased resulting in the poor efficiency.

2.3.2 Topology proposed by Ebrahimi et al (2014)

The topology proposed byEbrahimi et al utilizes m+1 power electronics switches and (m-1)/2 DC source to generate 2s+1 levels at the output (refer table 3a). By comparing this topology with conventional topology, a number of power electronics switches and DC sources used to generate output get reduced. Due to the reduction of number of power electronic switches and DC voltage sources, efficiency get improved compared to conventional topology.

2.3.3 Topology proposed by Ajami et al (2014)

The topology proposed byAjami et al requires ((m-1)/2) + 4 power electronics switches and (m-1)/2 DC source to generate 2s+1 levels at the output (refer table 3a). This topology requires a lesser number of power electronic switches and DC sources compared to the conventional topology and the topology proposed by Ebrahimi et al.(2014)

2.3.4 Proposed topology

The Proposed topology utilizes m-1power electronics switches and (m-1)/3 DC source to generate 3s+1 levels at the output (refer table 3a). Comparing the proposed topology with conventional topology and other proposed topologies, it is clear that the number of power electronics switches and DC sources used to generate output comparatively get reduced. The efficiency of the proposed topology is high compared to conventional topology and other proposed topologies. The proposed topology can be used in the applications such as drives and control of the electrical machine, connection of renewable resourcesetc.

Table 3b shows the comparison among the proposed topology, conventional topology and other topologies by substituting the value of m as 7. From the table, it is clear that the number of power electronics switches and DC sources used to generate seven levels at the output get reduced in case of proposed topology.

Table 3a Comparison table for 'm' level inverter

Components	Conventionaltopology	Ebrahimi et al	Ajami et al	Proposed topology
Main switching device	2(m-1)	m+1	((m-1)/2) + 4	m-1
Main diodes	2(m-1)	m+1	((m-1)/2) + 4	m-1
DC sources	(m-1)/2	(m-1)/2	(m-1)/2	(m-1)/3
Output levels	2s+1	2s+1	2s+1	3s+1

m represents number of output voltage levels.
s represents the separate DC voltage source.

Table 3b Comparison table for seven level inverter

Components	Conventionaltopology	Ebrahimi et al	Ajami et al	Proposed topology
Main switching device	12	8	7	6
Main diodes	12	8	7	6
DC sources	3	3	3	2
Output levels	7	7	7	7

3. Results and discussion

3.1 MATLAB simulation and results

In MATLAB, the simulation is done in the Simulink model and the MATLAB code is generated as per the switching pattern. The switching pulses for the cascaded multilevel inverter are generated by comparing the sine wave with the high-frequency triangular wave. The sine wave is taken as the reference wave and it is compared with the (n-1) high-frequency triangular waves to generate switching pulse to the proposed cascaded multilevel inverter circuit. Here 'n' denotes the number of output levels. The circuit is simulated with R load.

Figure 3 shows the switching pulses for the cascaded H-bridge multilevel inverter. The switching pulses thus produced are given to the six switches as the switching signals.

3.2 Xilinx simulation and results

The Xilinx ISE is primarily used for circuit synthesis and design while ISIM or the ModelSim simulator is used for system-level testing. As like MATLAB, the program is done in Xilinx ISE and it is executed in the ModelSim simulator. The program is done inthe form of VHDLcoding.

Figure 4 shows the switching pulses to six switches obtained by Xilinx simulation. The pulse thus obtained is similar to the pulse obtained by the MATLAB simulation.

3.3 Output of proposed topology

The result of the simulation is shown in the figures 5. The gate pulses obtained as a result of the simulation is given as an input to the switches. For example, if the maximum output voltage is 30. This is obtained due to the input dc voltage source values VL1=10, VR1= 20. Output levels are [30 20 10 0 -10 -20 -30].

4. Conclusion

The cascaded H-bridge multilevel inverter designed can generate seven levels at the output due to developed H-bridge circuit. From the description of existing topology and proposed topology, it is easy to understand the concept behind the conventional H-bridge and developed H-bridge. From the above results, it is clear that the number of power electronics devices used to build the inverter circuit gets reduced in the proposed inverter topology.

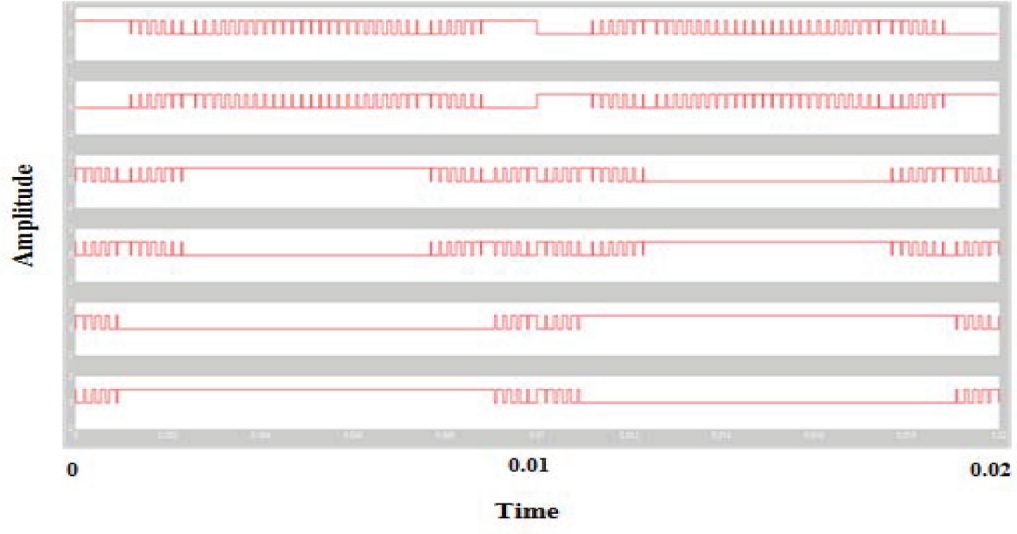

Figure 3 pulses generated in MATLAB

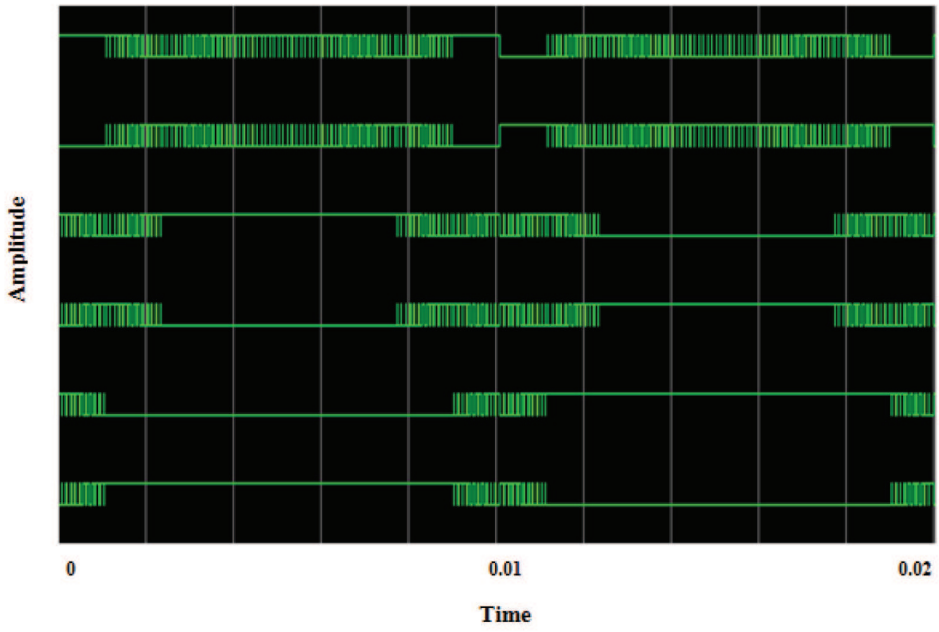

Figure 4 Pulses generated in XILINX

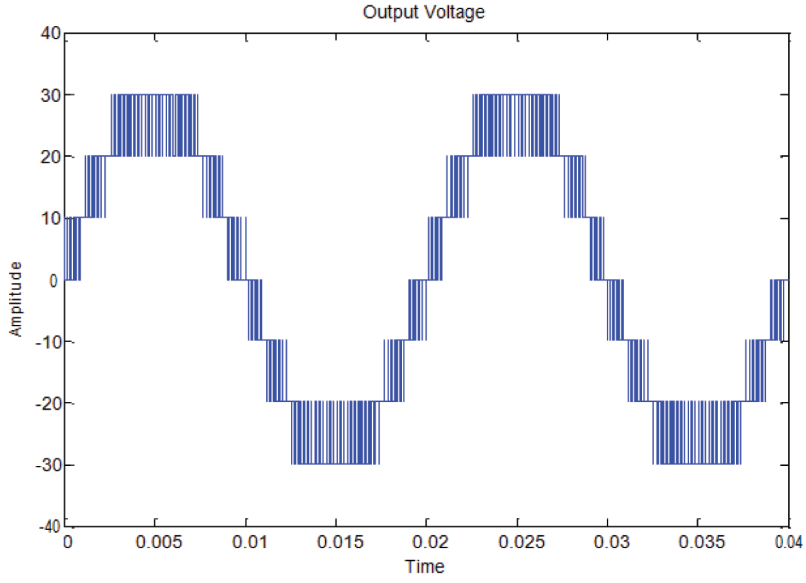

Figure 5 Waveform of 7- level inverter

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