An official publication of the International Society for Energy, Environment and Sustainability (ISEES)

Journal of Energy and Environmental Sustainability

Journal homepage : www.jees.in

Design and Simulation of Five Levels Active Neutralpoint Clamped Inverter

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ARTICLE INFO

Received : 04 September 2017
Revised : 09 November 2017
Accepted : 22 November 2017

Keywords:
Multi-Level Inverter (MLI), Active-Neutral-Point Clamped (ANPC) inverter, Flying-Capacitor, Total Harmonic Distortion (THD).

ABSTRACT

Multi-Level Inverters (MLI) are receiving more attentions nowadays as one of the preferred solutions for medium and high power applications. The Five-Level Active-Neutral-Point-Clamped inverter (5L-ANPC) combines the features of the conventional Flying-Capacitor (FC) type and Neutral-Point-Clamped (NPC) type inverterand is commercially used for industrial applications. The inverter configurations of Eight Switch Five Level Active Neutral Point Clamped (8S-5L-ANPC) inverter and Seven Switch Five Level Active Neutral Point Clamped (7S-5L-ANPC) inverter are discussed. The modulation strategy for 8S-5L-ANPC inverter is investigated and the results are presented. It is found that Total Harmonic Distortion (THD) of output voltage of 8S-5L-ANPC becomes 28.87%.

1. Introduction

Now a day's many industrial applications viz., compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro pumped storage, wind energy conversion, and railway traction etc.have begun to require high power. Few industrial loads such as drives require medium power for their operation. Using a high power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads (Teymour et al, 2015).The need of multilevel converter is to give a high output power from medium voltage source (Kouro et al, 2010).

The five-level inverter is a good choice for industrial application because of low Total Harmonic Distortion (THD), reduced switching stress and hence lower switching losses compared to the three-level inverter(Solution et al, 2009). However, conventional Five-Level NPC (5L-NPC) inverter, usethree clamping points in the DC-link. The control strategy to keep balanced voltage in each clamping point is difficult. Additionally, reverse recovery currents from clamping diodes will increase the switching losses of the system (Wang et al, 2015).The increased number of capacitors leads to increased volume of the system as well as complex control method to balance the voltages of both DC-link capacitors and FCs (Kashihara and Itoh, 2011).

Most popular hybrid MLI topology is the 5L-ANPC which combines a Three Level ANPC (3L-ANPC) leg with a 3L-FC power cell (Jiao and Lee, 2015). This topology enables the modularity factor, which islacking in the NPC type inverter by adding the FC power cell to reach higher level without adding series-connected diodes. Additionally, the 5L-ANPC inverter splits the DC-link into two capacitors (C1, C2), hence it is simpler to achieve voltage balance between these capacitors. Due to the reduced costs, volume and control complexity, the 5L-ANPC inverter has gained increasing attention recently and is already commercially used for medium power level industrial applications (Li and Huang, 2009).

2. Methods

2.1 Inverter Configurations

2.1.1 8$-5l-ANPC Inverter

The ANPC inverter produces five distinct output voltage levels by combining the three-level characteristic of the input stage (Cell 1) with the two-level of the output parts (Cell 2 and Cell 3as shown in Figure 2.1. The output voltage levels are achieved from eight distinct switching combinations, indicated by the combination of the switching functions of S1, S3 and S5 in Table I. It is understood that the switches S5 and S7 are operated in the same way and complementarily to S6 and S8.

The voltage level –Vdc/4 is generated either by the switching state F of G. Nevertheless, they cause an opposite effect on the floating capacitor voltage, due to the different combination of the switches. For a positive output phase current state G discharges, state F charges the floating capacitor (Serpa et al, 2008). Depending on the direction of the output phase current, these states have the ability to charge or discharge the

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floating capacitor. Besides that, the redundant combinations have also different impact on the mid-point potential, depending on the switching state of the input stage. For building an output voltage equal to –Vdc/4, the input stage can be connected either to the negative potential –Vdc/4 (G) or directly to M (F).

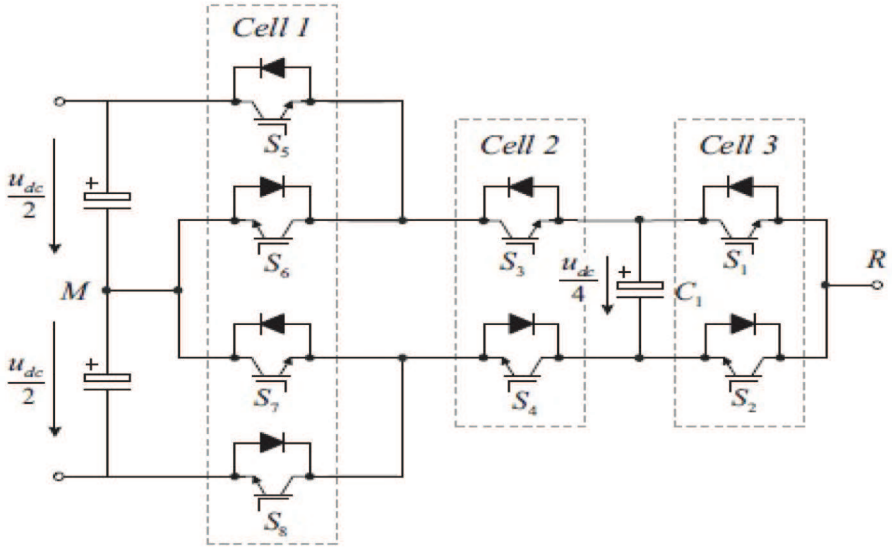

Figure 2.1 Circuit Diagram of 8S-5L-ANPC Inverter

Table I Switching States and Output Levels of 8S-5L ANPC Inverter

Switching State	S1	S2	S3	S4	S5	S6	S7	S8	Output Voltage Level
A	1	0	1	0	1	0	1	0	+2 (+Vdc/2)
B	0	1	1	0	1	0	1	0	+1 (+Vdc/4)
C	1	0	0	1	1	0	1	0	+1 (+Vdc/4)
D	0	1	0	1	1	0	1	0	0
E	1	0	1	0	0	1	0	1	0
F	0	1	1	0	0	1	0	1	-1 (-Vdc/4)
G	1	0	0	1	0	1	0	1	-1 (-Vdc/4)
H	0	1	0	1	0	1	0	1	-2 (-Vdc/2)

2.1.2 7S-5L-ANPC

In the 7S-5L-ANPC configuration, the DC-link consists of two series-connected capacitors (C1, C2), whose voltages are rated at half of DC voltage Vdc/2. A FC Cfc is required to provide one quarter of DC voltage (Vdc/4). Therefore, five output voltage levelsviz., +Vdc/2, +Vdc/4, 0,-Vdc/4 and -Vdc/2 (which are defined as +2, +1, 0, -1 and -2 respectively). The DC neutral point O is connected to both ends of the FC P and Q through two pairs of series connected switches and T type switches respectively, both of which require four active switches.

To decrease the number of active switches, four inner switches (T5 – T8) are ignored at first, as shown in Fig. 2.2 (a). When switches (T1, T2) or (T3, T4) are switched on, the inverter is generating +2 or -2 output levels (Hongliang Wang et al, 2016). Similarly, for the switching states which generate +1 or -1 levels, (T1, T3) or (T2, T4) are turned on. Both switching states are charging the FC under unity power factor condition. To keep the FC voltage balanced, additional two switching states which also generate +1 and -1 level to discharge the FC are required, which are called redundant switching states. To achieve this, the FC alone should be connected to output ends to provide the energy and the FC is discharging in these intervals. So for the redundant +1 level switching state, point P is connected to output point A through T2 while additional switches are needed to connect point O to Q. The direction of active current in this situation is from O to Q through FC and then from P to A, so additional active switch Ta and discrete diode Da are added, as shown in Fig. 2.2 (b). The reason for adding Da is to prevent FC being directly connected to C1 when T1 is on. However, the main current branch should be bi-directional, thus to obtain the reactive current path, additional switch Tb and diode Db are added in parallel with Da. The reactive current will flow through Ta, Tb and Db. It is understood that the circuit in Fig. 2.2 (b) is also capable of generating 0 level when newly added branch and T3 are on. Similarly, in Fig. 2.2 (c), two active switches Tc, Td and two discrete diodes Dc, Dd are added to provide redundant -1 and 0 level switching states (Tb and Td), (Db and Dc), (Da and Dd) can be merged as shown in Fig. 2.2 (d).

The function of T7 is to provide bi-directional current paths for O to P and O to Q. Two discrete diodes D7 and D8 act as the body diode of switch T7 to limit the reverse voltage, so that the selection of T7 can be IGBT without anti-parallel diode thus, reducing the system cost.The switching states and the output levels are given in the Table II.

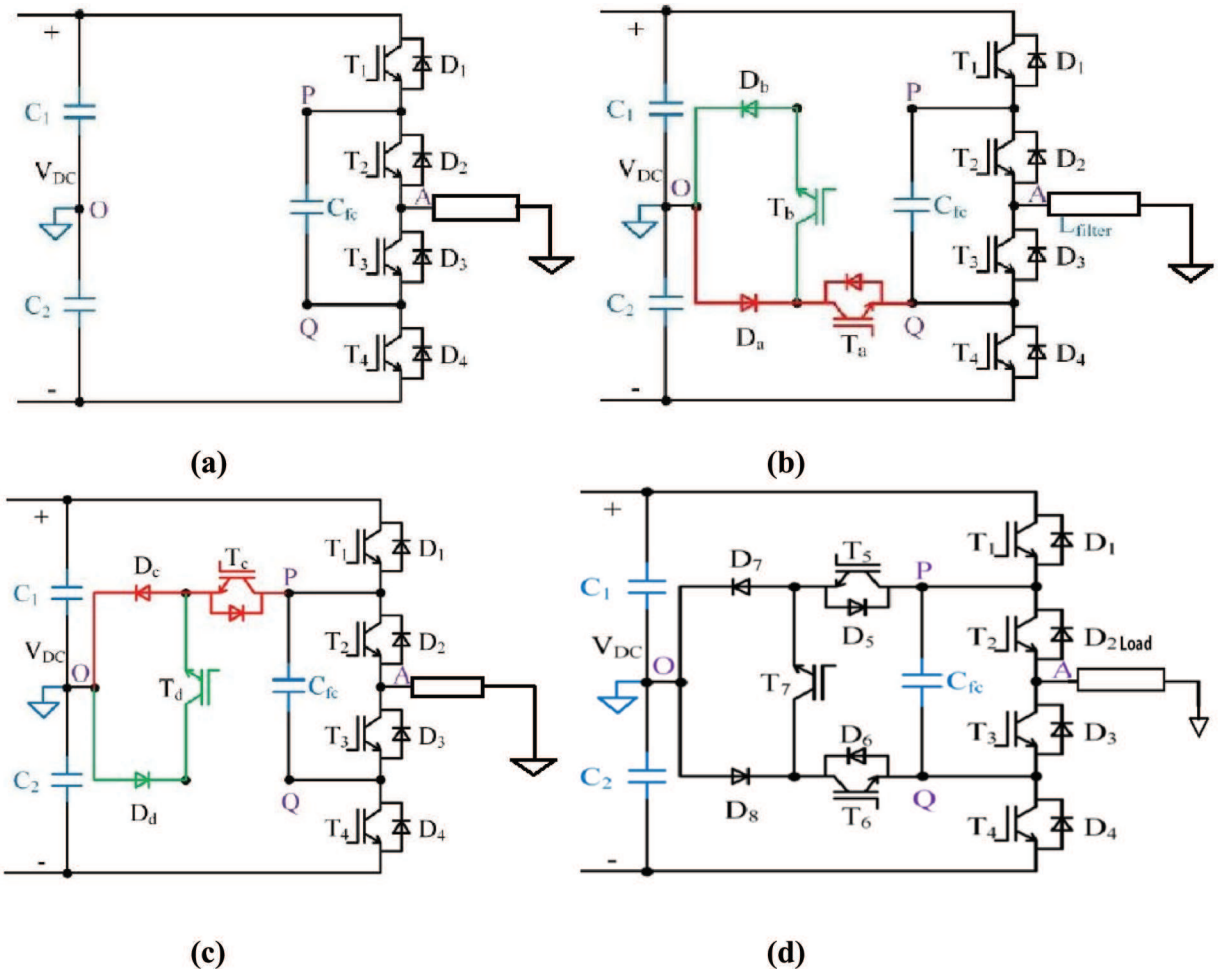

Figure 2.2 (a) Circuit 1. (b) Circuit 2. (c) Circuit 3. (d) Proposed Topology

Table II Switching States and Output Levels of 7S-5L-ANPC Inverter

Switching State	T1	T2	T3	T4	T5	T6	T7	Output Voltage Level
A	1	1	0	0	0	1	0	+2 (+Vdc/2)
B	1	0	1	0	0	1	0	+1 (+Vdc/4)
C	0	1	0	0	0	1	1	+1 (+Vdc/4)
D	0	0	1	0	0	1	1	0
E	0	1	0	0	1	0	1	0
F	0	0	1	0	1	0	1	-1 (-Vdc/4)
G	0	1	0	1	1	0	0	-1 (-Vdc/4)
H	0	0	1	1	1	0	0	-2 (-Vdc/2)

2.2 Control Algorithm for 8S-5L-ANPC

The switching schemeof 5L-ANPCincludes four carrier waves of frequency 15 kHz and the sinusoidal reference waveform of 50 Hz are depicted in the Figure 2.3. The firing pulses associated with switching states A, B, D, G and H (listed in Table I) are generated based on comparing reference voltage with respective carrier signals. Moreover, redundant switching states of D and E are used to reduce the switching frequency. The program for the generation of pulses to the gates is fed to the interpreted MATLAB function. The output from the function block is given to the eight IGBT switches.

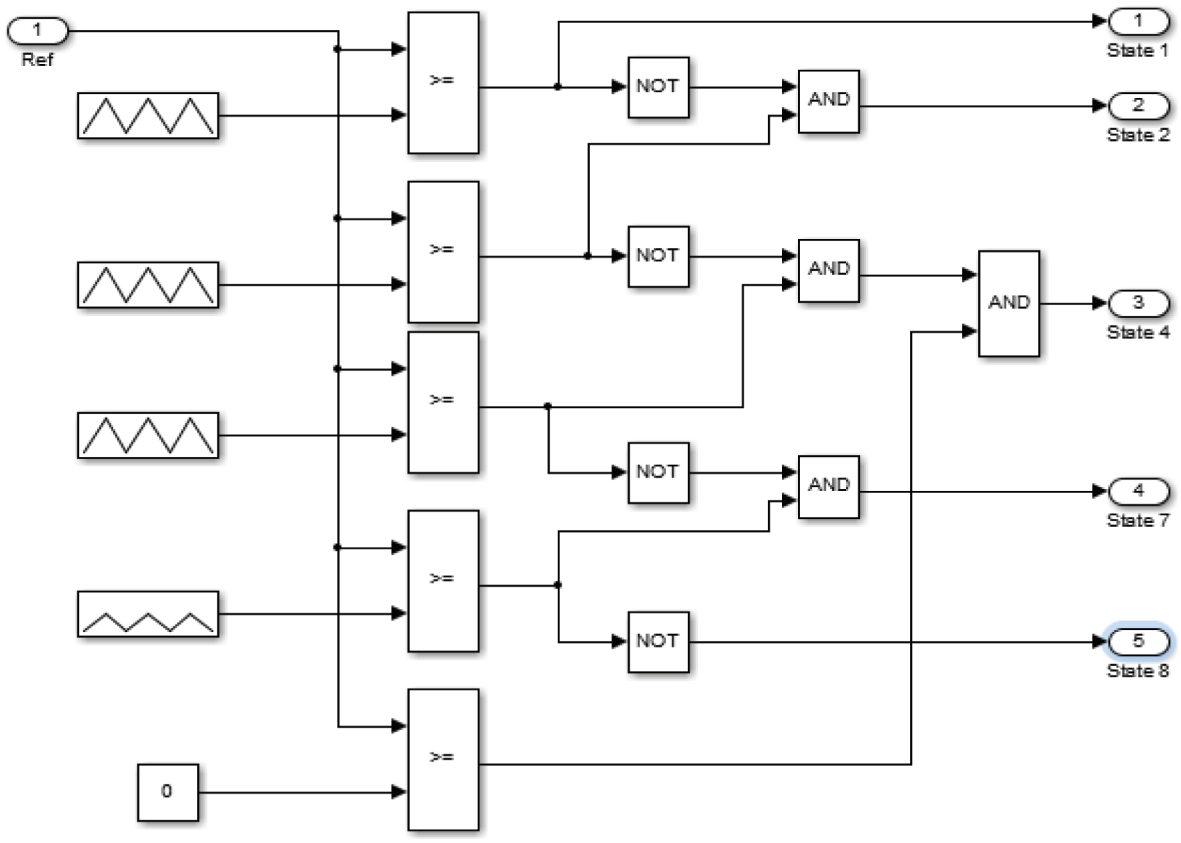

Figure 2.3 Generation of Gate Pulses for 5L-ANPC Inverter

2.2.1 Pseudo Code for the Control Algorithm

```
function [y]= xx(x)
a=x(1);b=x(2);c=x(3);d=x(4);e=x(5);
if a>0
        y1=1;y2=0;y3=1;y4=0;y5=1;y6=0;y7=1;y8=0;
elseif b>0
        y1=0;y2=1;y3=1;y4=0;y5=1;y6=0;y7=1;y8=0;
elseif c>0
        y1=0;y2=1;y3=0;y4=1;y5=1;y6=0;y7=1;y8=0;
elseif d>0
        y1=1;y2=0;y3=0;y4=1;y5=0;y6=1;y7=0;y8=1;
elseif e>0
        y1=0;y2=1;y3=0;y4=1;y5=0;y6=1;y7=0;y8=1;
else
        y1=1;y2=0;y3=1;y4=0;y5=0;y6=1;y7=0;y8=1;
end
        y=[y1,y2,y3,y4,y5,y6,y7,y8];
```

3. Results and Discussion

The 5L-ANPC inverter is simulated using MATLAB/Simulink software. The Table III shows the system parameters considered for the simulation.

Table III System Parameters

Parameter	Values
DC-link voltage	400 V
DC Capacitance	1500μF each
Flying Capacitance	1000μF
Switching Frequency	15 kHz
Resistance Load	200 Ω

The inverter circuit supplied with input voltage of 400V. The gate pulses generated by using open loop switching algorithm as shown in Figure 3.1. The output voltage is measured across the 200 Ω load. The output voltage waveform is shown in Figure 3.2. By selecting the correct redundant switching state the voltages of the three floating capacitors are controlled to Vdc/2.

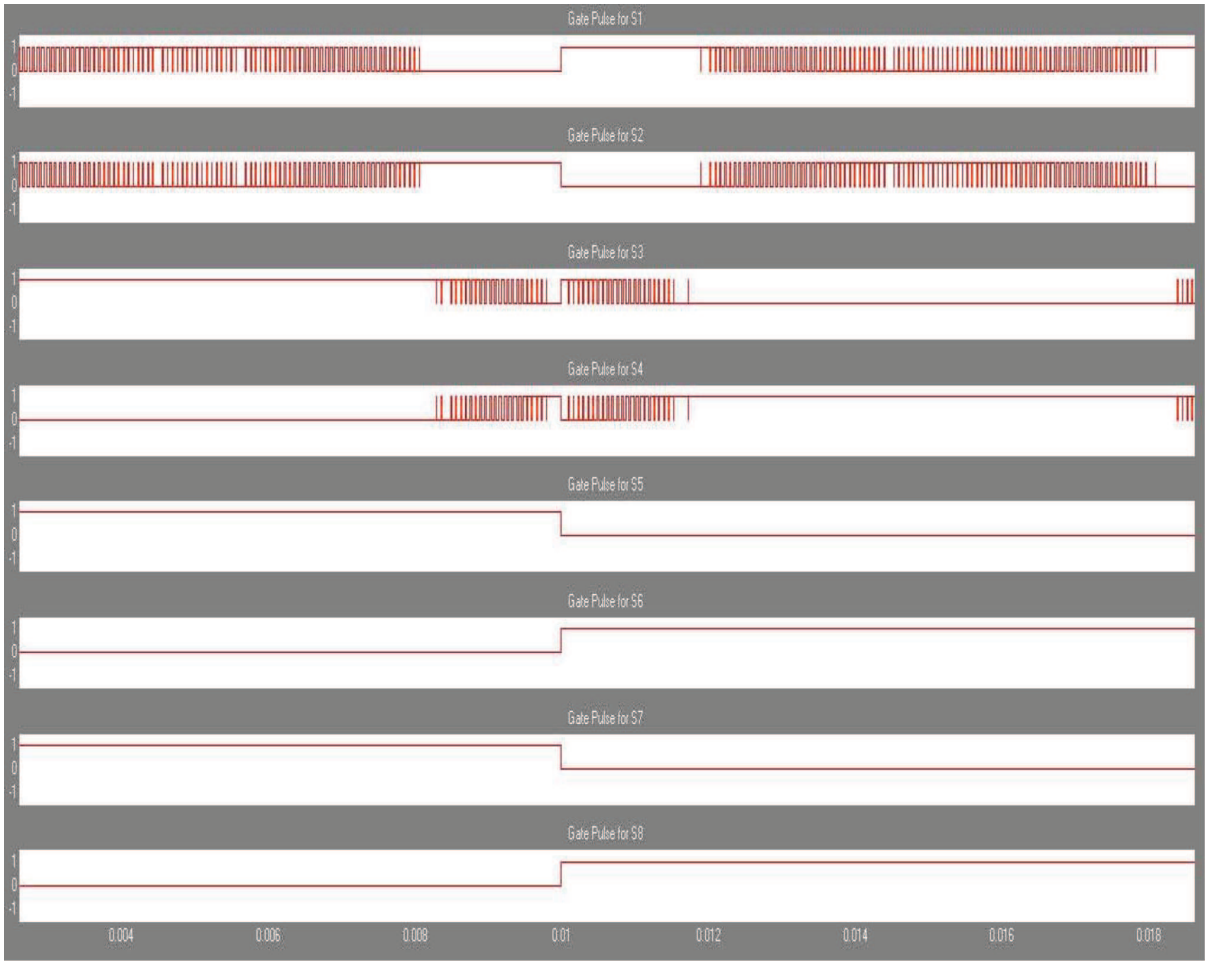

Figure 3.1 Gate Pulses for 5L-ANPC Inverter

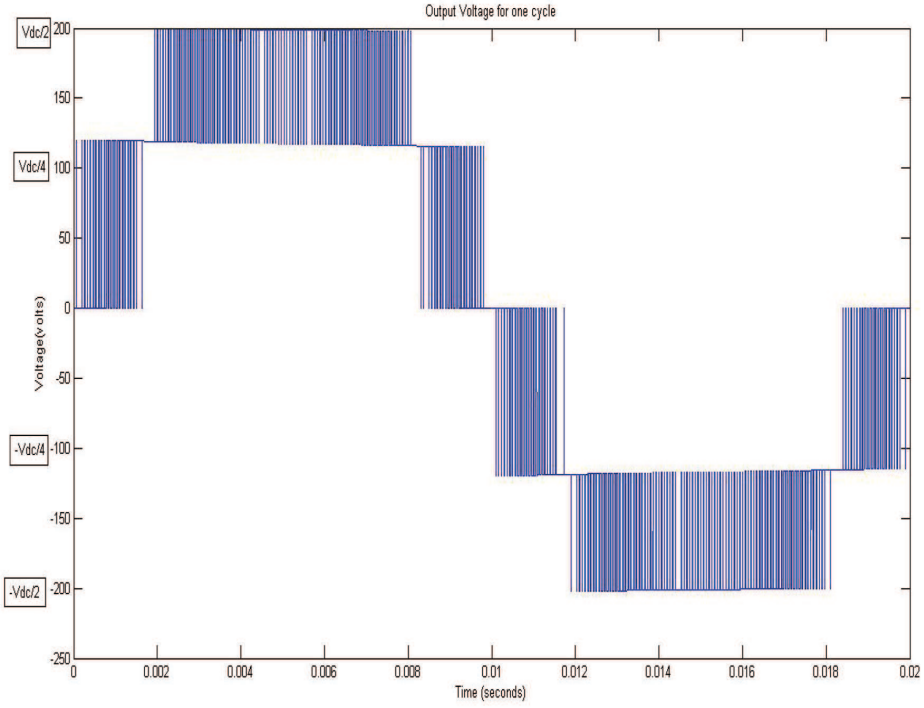

Figure 3.2 Output Voltage Waveform for one cycle of 8S-5L-ANPC Inverter

The THDfor the Optimum Pulse Width Modulation (PWM)control scheme of five level MLI comes out to be 30.31% (Li J and Huang A Q, 2009). The THD of 5L-ANPC with open loop switching algorithm is found to be 28.87 % asshown in the Figure 3.3.

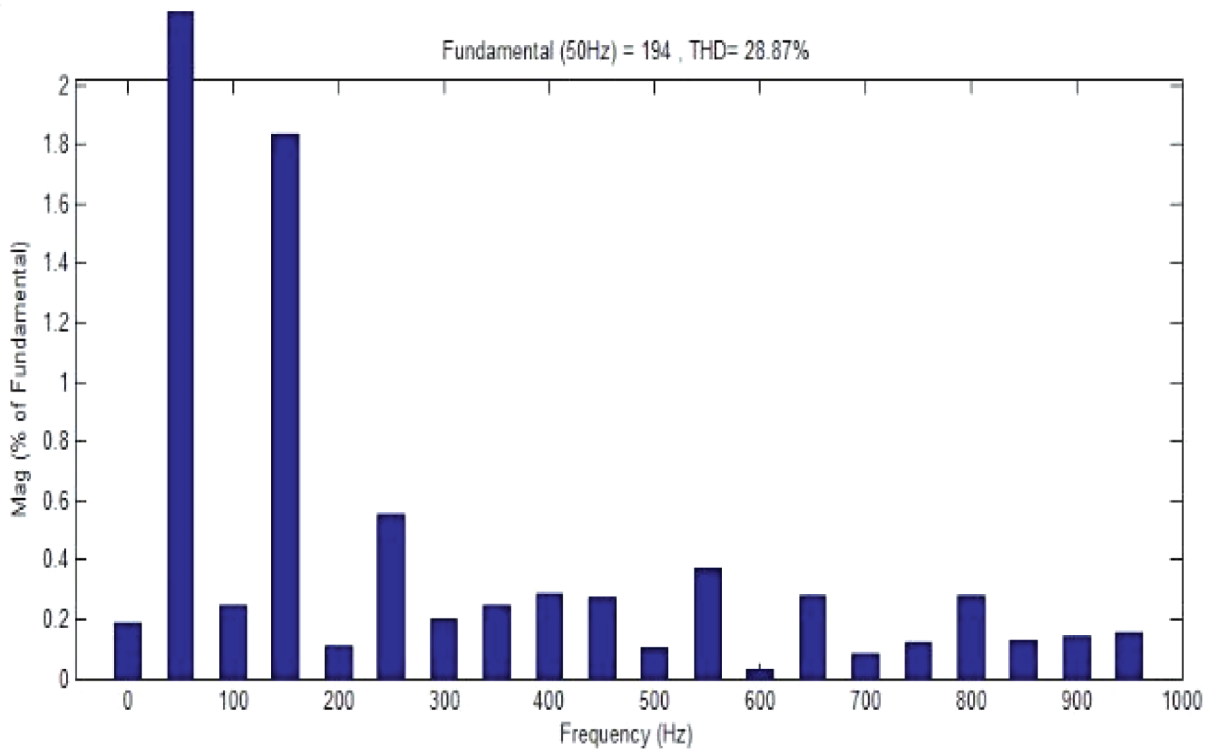

Figure 3.3 THD of 5L-ANPC Inverter

4. Conclusion

The switching states of five level active neutral point clamped inverter is analyzed and simulated using MATLAB/Simulink. The gate pulses for 8S-5L-ANPC Inverter is generated using open loop switching algorithm and the output voltage signals are plotted.The THD of 8S-5L-ANPC is reduced from 30.31% to 28.87%. The comparative analysis of 8S-5L-ANPC and 7S-5L-ANPC inverters will be published.

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